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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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BAKER & MCKENZIE
PATENT DEPARTMENT
2001 ROSS AVENUE
SUITE 2300
DALLAS, TX 75201

EXAMINER	
NGUYEN, LONG T	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 03/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/765,966	BU ET AL.	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 January 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This office action is responsive to the amendment filed on 1/7/05.

Specification

2. The disclosure is objected to because of the following informalities: there is no description for newly added Figure 5B in the specification. Note that the specification only describes original Figure 5, and the specification was not amended to address the changes of Figure 5 to Figure 5A, and newly added Figure 5B. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 11, 15 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirano (USP 6,433,582).

With respect to claim 1, Figure 2 of the Hirano reference discloses a level-shifter circuit for shifting a signal (Si) of a first logic family at a first lower voltage level (Vcc) to a second higher voltage level (Vpp) for a second logic family, the level shifter circuit includes: a first PMOS (P1), a first NMOS (N1), a second PMOS (P2), a second NMOS (N2), a power-down control PMOS (PR1); means (ADT circuit, see Figure 4) for supplying a power-down control signal (ATD) to the gate of the power-down control PMOS (PR1), the power control signal being

changed to a high state for a predetermined period of time when the signal (Si) from the first logic family changes state (timing diagram in Figure 3 shows that when the input signal Si changes state, the power down signal ATD is Hi for a period of time), and the shifted output (T2, T3).

With respect to claims 11, 15 and 16, these claims are rejected for the similar manner as discussed above with regard to the rejection on claim 1. Note that Figure 2 shows a level shifter including a level shift unit (P1, P2, N1, N2, INV1) including an input terminal (T1) and an output terminal (T2), a power terminal (Vpp), a first transistor (PR1). Note that the level shift unit is a level-up shift device because it shifts a lower voltage Vcc to a higher voltage Vpp.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2, 3 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 6,433,582) in view of Kim (USP 5,917,339).

With respect to claim 2, the level shifter in Figure 2 of the Hirano reference meets all the limitations of this claim except that the level shifter including first and second inverters connected in series to the output for providing a pair of complementary output signal. However, the Kim reference discloses in Figure 2 a level shifter circuit including first and second inverters (15-16) connected in series and connected to the output for the purpose of buffering the output signal for output driving (i.e., driving downstream circuitry). Therefore, it would have been

obvious to one having skill in the art that the time the invention was made to modify the circuit in Figure 2 of the Hirano reference by providing series-connected first and second inverters to each of the outputs T2 and T3 of the level shifter circuit for the purposes of buffering the output signal to improve the driving capability of the output signal (i.e., providing two inverters connected in series with the output terminal T2, and providing another two inverters connected in series with the output terminal T3 in Figure 2 of Hirano). Thus, this modification meets all the limitations of claim 2. Note that, with such modification/combination, the output of the first inverter and the output of the second inverter of the two inverters connected in series with the output terminal T2 provides the pair of complementary of the output signal; and similarly, the output of the first inverter and the output of second inverter of the another two inverters connected in series with the output terminal T3 provides another pair of complementary of the output signal.

With respect to claim 3, the modification as discussed in claim 2 meets all the limitations of this claim, i.e., this claim is rejected for the same manner as in claim 2.

With respect to claim 17, this claim is rejected for the similar manner as in claim 2 which discussed above. Note that the first transistor is the power down control transistor PR1.

7. Claims 4-9 and 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 6,433,582) in view of Kim (USP 5,917,339) and further in view of Tanaka et al. (USP 6,249,145).

With respect to claim 4, the modification/combination (Hirano and Kim) as discussed above with regard to claim 3 meets all the limitation of this claim except that the level shifter circuit including a third NMOS transistor connected between the gate of the first PMOS

transistor and ground. However, Figure 12 of the Tanaka et al. reference shows a level shifter circuit (516) including a third NMOS transistor connected between the gate of first PMOS transistor 300 and ground and is controlled be the same power-down control signal for the purpose of stabilizing the output of the level shifter at a predetermined level during the power-down control PMOS transistor (314, Figure 12 of Tanaka et al.) is off. Therefore, it would have been obvious to one having skill in the art that the time the invention was made to modify the above combination/modification (Hirano and Kim) by providing each of the output nodes nd1 and nd4 (Figure 2 of Hirano) with a third NMOS transistor connected between the respective nodes nd1 and nd4 (gates of PMOS transistors P2 and P1) and ground for the purpose of stabilizing the output of the level shifter circuitry at a predetermined voltage level during the power control PMOS transistor of the level shifter is off, and thus reducing the power consumption of the circuitry. Thus, this modification/combination meets the limitation that the level shifter circuit including a third NMOS transistor connected between the input of the first inverter and ground (i.e., connected between node nd4 in Figure 2 of Hirano and ground).

With respect to claim 5, the combination/modification as discussed in claim 4 above meets the limitation that the level shifter circuit including a resistor (i.e., the third NMOS transistor as discussed above. Note that a MOSFET acts as a variable resistor due to the signal at the gate of the MOSFET controlling the resistance of the MOSFET).

With respect to claim 6, this claim is rejected for the same manner as in claim 4.

With respect to claim 7, the combination/modification (Hirano, Kim and Tanaka et al.) as discussed in claim 6 meets all the limitations of the claim except that the level shifter including a third PMOS transistor connected between the power supply terminal and the power-down control

PMOS transistor. However, Figure 6 of the Tanaka et al. reference discloses a level shifter circuit including a PMOS transistor (306) connected between the power supply terminal (VDDQ) and the cross-coupled PMOS transistors of the level shifter for the purpose of ensuring the corrected operation of the circuitry under low power application (Col. 6, line 25-48 of Tanaka et al.). Therefore, it would have been obvious to modify the above combination/modification (claim 6) by providing a third PMOS transistor directly connected to the power supply terminal and between the power-down control PMOS transistor (i.e., connected a PMOS transistor 306 in Figure 6 of Tanaka et al. between the power terminal Vpp and the power-down PMOS PR1 in Figure 2 of the Hirano reference in the above combination/discussion of claim 6) for the purpose of ensuring the corrected operation of the level shifter under lower power application and thereby reducing power consumption. Thus, this modification meets all the limitations of claim 7.

With respect to claim 8, the modification discussed in claim 7 also meets the limitations of claim 8, i.e., claim 8 is rejected for the same manner as in claim 7.

With respect to claim 9, the third PMOS transistor as discussed in claim 7 (i.e., transistor 306) is a constant source.

With respect to claims 18-20, the modification discussed in claims 4 and 5 meet all the limitations of these claims. Note that the "second transistor" in claim 18 is the third NMOS transistor discussed in claim 4 above; the resistor is also the third NMOS transistor (variable resistor) as discussed in claim 5; and the first and second inverters are the inverters discussed in claim 4.

8. Claims 8 and 9 are also rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 6,433,582) in view of Tanaka et al. (USP 6,249,145).

With respect to claim 8, the level shifter circuit in Figure 2 of the Hirano reference meets all the limitations of the claim (similar as discussed in claim 1 in the 102 rejection) except that the level shifter including a third PMOS transistor connected between the power supply terminal and the power-down control PMOS transistor. However, Figure 6 of the Tanaka et al. reference discloses a level shifter circuit including a PMOS transistor (306) connected between the power supply terminal and the cross-coupled PMOS transistors of the level shifter for the purpose of ensuring the corrected operation of the circuitry under low power application (Col. 6, line 25-48 of Tanaka et al.). Therefore, it would have been obvious to modify the level shifter in Figure 2 of the Hirano reference by providing a third PMOS transistor directly connected to the power supply terminal and between the power-down control PMOS transistor (PR1, Figure 2 of Hirano) for the purpose of ensuring the corrected operation of the level shifter under lower power application and thereby reducing power consumption. Thus, this modification meets all the limitations of claim 8.

With respect to claim 9, the third PMOS transistor as discussed in claim 8 (i.e., transistor 306) is a constant source.

9. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 6,433,582).

With respect to claim 10, Figure 2 of the Hirano reference discloses a level shifter circuit (as discussed in claim 1) which having the structure for shifting positive power supply voltage. The different between the prior art (Figure 2 of Hirano) and the claim invention is that the

structure of the claim invention is for shifting the negative power voltage instead of shifting the positive power voltage. However, it is notoriously well-known that a circuit operates with positive power supply voltage can be modify to operate with negative power supply voltage by replacing each NMOS transistor in the circuit with a PMOS transistor, and each PMOS transistor in the circuit with an NMOS transistor. Therefore, it would have been obvious to one having skill at the time the invention was made to modify the circuit in Figure 2 of Hirano by replacing each NMOS transistor in the circuit with a PMOS transistor, and each PMOS transistor in the circuit with an NMOS transistor for the purpose of operating the circuit with a particular power supply depending on the need of the designer (i.e., negative power supply in this case). Note that, in this modification, the power supply Vpp is now a negative power supply. Thus, this modification meets all the limitations of claim 10 as it can be seen that the modification circuit (i.e., replacing each NMOS transistor in the circuit in Figure 2 with a PMOS transistor, and each PMOS transistor in the circuit with an NMOS transistor) including: a first PMOS (the NMOS N1 as shown in Figure 2 becomes a first PMOS), a first NMOS (the PMOS P1 in Figure 2 becomes a first NMOS), a second PMOS (a second NMOS N2 in Figure 2 becomes a second PMOS), a second NMOS (a second PMOS P2 in Figure 2 becomes a second NMOS), a power-down control NMOS (power-down control PMOS PR1 become a power-down control NMOS); the shifted output (T2, T3), and the power control signal (ATD). Note that because power down control signal (timing diagram in Figure 3 of Hirano) in this modification must therefore changes to a low state when the input signal of the level shifter changes state due to the reversal in the modification (i.e., positive changes to negative, PMOS to NMOS and vice versa, so logic Hi in timing diagram of Figure 3 must become logic Lo)..

10. Claims 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano (USP 6,433,582) in view of Tanaka et al. (USP 6,249,145).

With respect to claim 12, Figure 2 of the Hirano reference discloses a level shifter as discussed above with regard to claim 11 meets all the limitation of this claim except that the level shifter circuit including a second transistor connected between the output terminal of the level shifter and ground. However, Figure 12 of the Tanaka et al. reference shows a level shifter circuit (516) including a third NMOS transistor connected between the output terminal of the level shifter 516 and ground and is controlled be the same power-down control signal for the purpose of stabilizing the output of the level shifter at a predetermined level during the power-down control PMOS transistor (314, Figure 12 of Tanaka et al.) is off. Therefore, it would have been obvious to one having skill in the art that the time the invention was made to modify the level shifter in Figure 2 of Hirano by providing each of the output nodes nd1 and nd4 (Figure 2 of Hirano) with an NMOS transistor connected between the respective output nodes nd1 and nd4 and ground for the purpose of stabilizing the output of the level shifter circuitry at a predetermined voltage level during the power control PMOS transistor of the level shifter is off, and thus reducing the power consumption of the circuitry. Thus, this modification/combination meets the limitation that the level shifter circuit including a second transistor which turns on to connect the output terminal of the level shifter unit to a predetermined voltage when the first transistor (power down PMOS PR1 in Figure 2 of Hirano) is off.

With respect to claim 13, the combination/modification as discussed in claim 11 above meets the limitation that the level shifter circuit including a resistor (i.e., the third NMOS transistor as discussed above -- note that a MOSFET acts as a variable resistor due to the signal

at the gate of the MOSFET controlling the resistance of the MOSFET) connected between the output terminal a predetermined voltage terminal (ground).

With respect to claim 14, the level shifter circuit in Figure 2 of the Hirano reference as discussed in claim 11 meets all the limitations of the claim except that the level shifter including a second transistor connected between the power supply terminal and the first transistor. However, Figure 6 of the Tanaka et al. reference discloses a level shifter circuit including a PMOS transistor (306) connected between the power supply terminal and the cross-coupled PMOS transistors of the level shifter for the purpose of ensuring the corrected operation of the circuitry under low power application (Col. 6, line 25-48 of Tanaka et al.). Therefore, it would have been obvious to modify the level shifter in Figure 2 of the Hirano reference by providing a second transistor directly connected to the power supply terminal (Vpp) and between the power-down control PMOS transistor (PR1, Figure 2 of Hirano) for the purpose of ensuring the corrected operation of the level shifter under lower power application and thereby reducing power consumption. Thus, this modification meets all the limitations of claim 11. Note that transistor 306 in Figure 6 of Tanaka et al. is a constant source.

Response to Arguments

11. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

12. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

13. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Friday from 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

February 22, 2005

Long Nguyen
Primary Examiner